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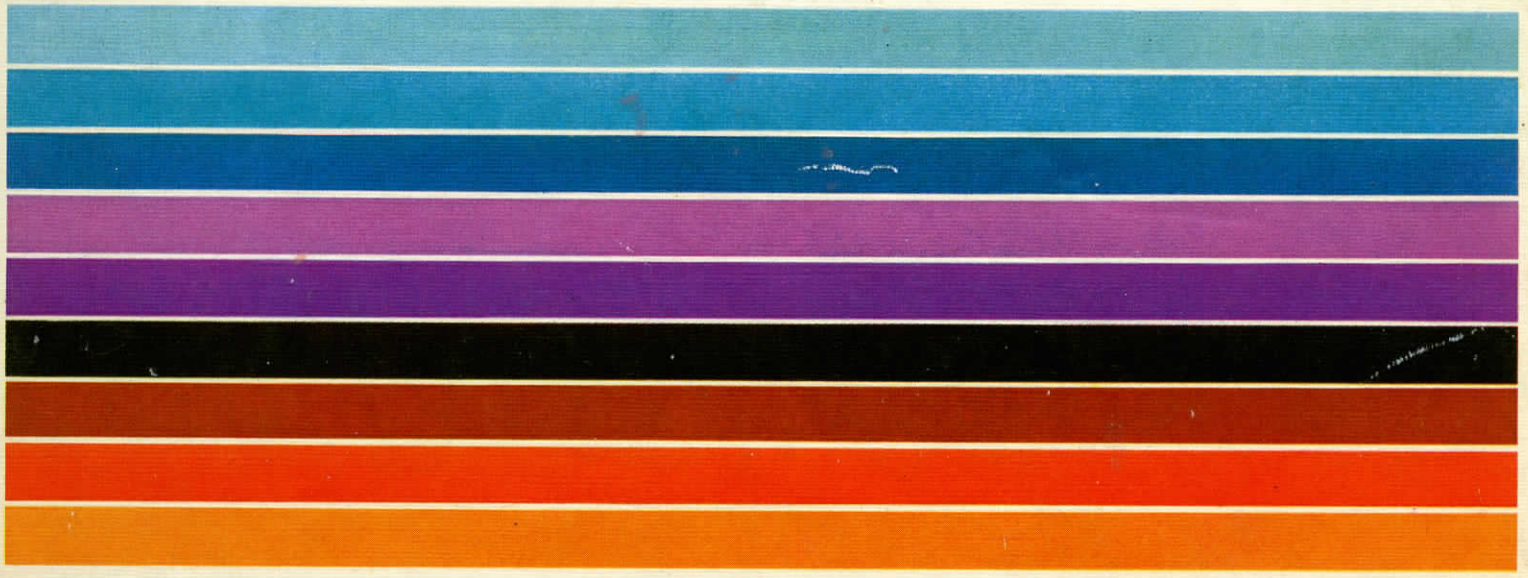
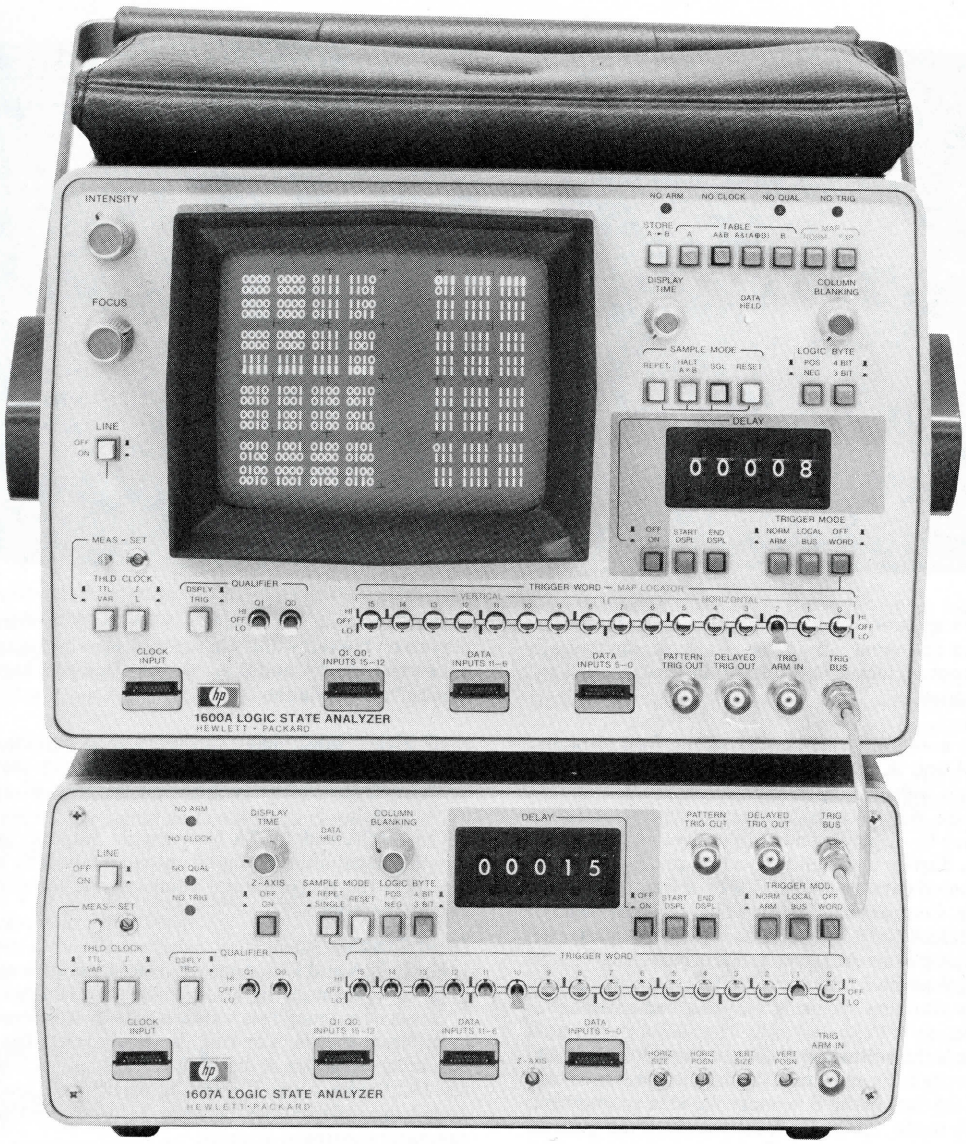
PACKARD

Measurement/Computation

ELECTRONIC INSTRUMENTS AND SYSTEMS 1980





1600S

1600S Description

The 1600S Logic State Analyzer is a versatile, general purpose data domain instrument for use in design and troubleshooting of minicomputer and microprocessor based systems as well as other digital systems. Parallel data is captured at clock speeds to 20 MHz and presented in an easy-to-read one's and zero's display format for fast functional analysis of digital data flow. The ability to capture and display words up to 32-bits wide lets you observe, in real time, microcodes or addresses with resulting data, saving time in system design and development, hardware troubleshooting, software evaluation, and service and maintenance. Convenient and flexible functional analysis is provided by features such as sequential triggering, dual clock, separately configured data tables, display qualification, exclusive OR comparison of Tables A and B, dynamic mapping, and halt when A is not equal to B.

The 1600S consists of a 1600A Logic State Analyzer, a 1607A Logic State Analyzer, a 10236A Trigger Bus Cable, and a 10237A Data Cable. The Trigger Bus Cable logically AND's the trigger registers of both the 1600A and 1607A for a trigger word up to 36 bits wide (four qualifiers not displayed). The Data Cable connects the 1600A Table B memory to the 1607A to enable the display of words up to 32 bits wide, to display two 16-bit data sequences at the same time—such as addresses and instructions, to display 32 consecutive 16-bit words, or for dual clock application. When the full system capabilities are not needed, the 1600A or 1607A may be used separately. The 1600A by itself is a complete logic state analyzer with 16-bit triggering plus two qualifiers, and a 32-bit wide table display as well as dynamic mapping. The 1607A needs only the proper oscilloscope or X-Y display for another complete analyzer, also with 16-bit triggering plus two qualifiers. Both the 1600A and 1607A have a pattern trigger output to trigger an oscilloscope for electrical analysis.

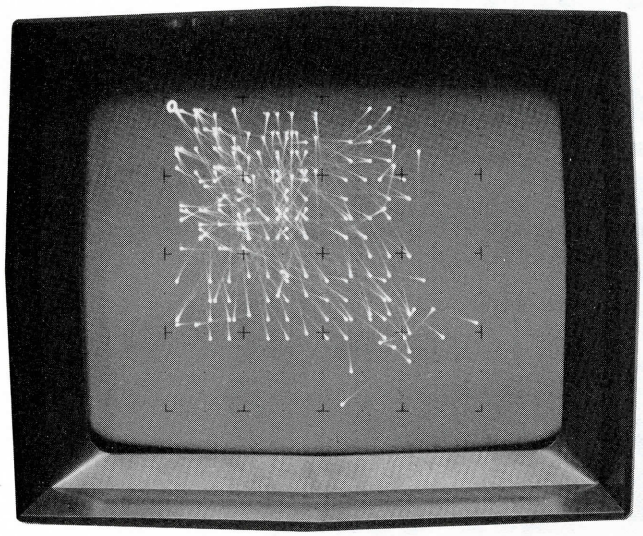
Display Modes

The Map display provides a dynamic overview of a system's operation—a pattern of dots interconnected with vectors that are unique for each area of program implementation. Each dot represents a specific word; its location indicates binary magnitude and its brightness indicates relative frequency of occurrence. The vectors between each dot allow you to observe the sequence of data transactions. The vector gets brighter as it moves toward a new point to show the direction of data flow. With the map you can identify program loops, improper data flow, as well as lost portions of a program. You can also map single-shot events such as those in turn-on sequences.

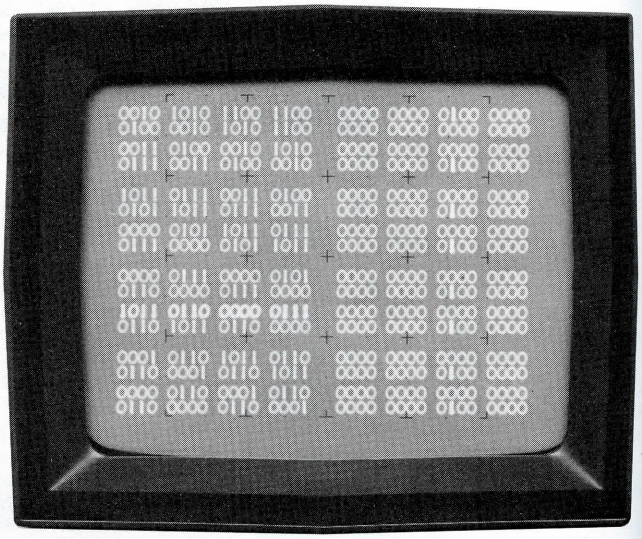
In the Table display mode you can display up to sixteen 32-bit words which allow you to view address and resultant data flow at the same time. You can look at events leading up to, surrounding, or following the trigger word; and delay up to 99 999 clock cycles beyond

LOGIC ANALYZERS

Models 1600S, 10253A & 10254A (cont.)



The map display offers an overall view of machine operation, with each dot representing one input word. The real time display allows you to identify program loops, improper data flow, as well as lost portions of a program.



In the Exclusive OR mode, A & (A ⊕ B), A memory data is displayed on the left while the table on the right displays logic differences between A and B memories. This provides very fast "at-a-glance" comparisons.

the trigger point to view events anywhere in a program. Two 16-bit by 16-bit table displays, A and B, can be used separately or in various combinations to satisfy a wide variety of applications.

An Exclusive OR mode, A & (A ⊕ B), makes comparison of Table A and Table B data easy by displaying any differences as intensified one's on Table B. This display mode allows you to quickly compare active data to known stored data, or to compare data from two active systems simultaneously. Comparison data for Table B can be entered from an HP Model 10253A Card Reader. Model 10253A plugs directly into the 1600A Logic State Analyzer and provides a convenient method for performing repetitive tests for incoming inspection, production testing, or any situation requiring frequent comparisons to predetermined data sets.

Another useful mode is the halt when A does not equal B mode (A ≠ B), which automatically halts and stores the data in the A memory when it does not equal the data in the B memory. Used in conjunction with the A & (A ⊕ B) mode, this mode frees you from the tedious waiting and watching for intermittent malfunctions.

Display Qualification and Triggering

The 1600S has a total of four qualifier channels which allow only selected data to be captured, greatly expanding the effectiveness of the memory since irrelevant or extraneous data is not strobed into memory. The 1607A pattern trigger output (PTO) can be used as a qualifier input to the 1600A for analysis of multiplexed buses.

You can define two events which must occur in sequence to trigger a data acquisition cycle. The trigger output of the 1607A can be used to arm the 1600A on a selected event, enabling it to look for the second event. Sequential triggering is useful for analyzing branch operations.

Both the 1607A and the 1600A may be operated in the Start Display or End Display modes. In Start Display, the Analyzer triggers on a unique word established by the trigger word switches and displays that trigger word and the fifteen following words as they are clocked in. This is a valuable mode for paging through a system while following an algorithm to trace data flow. End Display triggering captures events leading up to and including the trigger word, providing a "negative time" display. This is extremely helpful for troubleshooting, since you can trigger on an unallowed state or a fault and see where the machine malfunctioned rather than the end results of the error. In addition, delay may be combined with the End Display trigger to capture both positive and negative time data, allowing you to see events before and after the trigger event and reduce analysis time.

When the data you want to see does not immediately follow the desired trigger word, delay can be used to position the sixteen word "window" an exact number of clock pulses from the trigger word. The 1600A and the 1607A each permit selection of up to 99 999 clock cycles of delay.

The 1600A and 1607A have trigger outputs that extend troubleshooting capabilities in digital curcuit analysis by windowing oscilloscopes to the proper digital point in time for electrical analysis of circuit operation.

Dual Clock

The 1600A and 1607A may be clocked at different rates which permits you to examine simultaneously up to 16 bits on both sides of an I/O port even though state flow is from two different sources running at different speeds. You can also easily relate bus activity to events occurring elsewhere at different clock rates, such as system peripherals. Dual clock capability can be particularly useful in determining design incompatibilities between hardware and software in microcomputer-controlled systems.

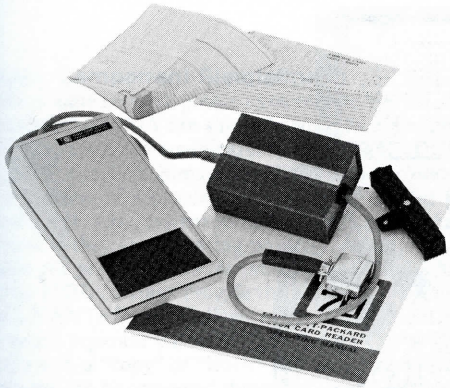
Serial Data Analysis

Model 10254A Serial-to-parallel Converter extends the analytical capabilities of the 1600S to include monitoring serially transmitted data. Data is collected serially at rates to 10 MHz into bidirectional registers and transmitted in parallel to the 1600S by bytes up to 16 bits wide. Sync mode may be a Pattern sync, initiating data collection with the pattern triggers of the analyzer, or Edge sync, using the appropriate edge of the clock for the system under test. You can use the Converter with either Model 1600A or Model 1607A and a display, or two Converters for a display of serial data 32 bits wide. Operating parameters are matched to those of the 1600S, including a zero hold time and adjustable threshold levels. With the 1600S and 10254A in combination, you can observe data transfers at I/O ports, and monitor communication networks, serial processors, and digital filters.

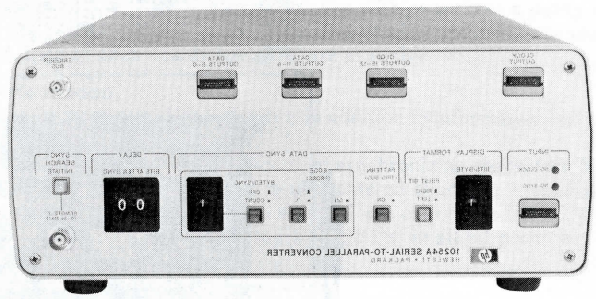
Versatile Miniature Probes

The 1600S acquires data through six, 6-channel high impedance probes. Two separate clock probes allow connection to the desired strobe source. The miniature probe tips are small enough to connect to adjacent pins or can be slipped off the probe wire for direct connection to 0.6 mm (0.025 in.) square pins, IC test clips, Model 10024A IC clip, and wire wrap pins.

Individual probes are connected to each data or clock pod through a quick disconnect ganging-bar which permits hardwired or semipermanent connections to system nodes that do not need to be disturbed when the Logic State Analyzer and its probe pods are removed.



10253A Card Reader



10254A

1600S Specifications

Clock and Data Inputs

Repetition rate: 0 to 20 MHz.
Input RC: 40 kΩ ± 3 kΩ shunted by ≤14 pF (at the probe tip).
Input bias current: ≤30 μA.
Input threshold: TTL, fixed at ≈ +1.5 V; variable ±10 Vdc.
Max input: level, −15 to +15 Vdc; swing, 15 V peak from threshold.
Min input: swing, 0.5 V +5% of p-p threshold voltage; clock pulse width, 20 ns at threshold; data pulse width, 25 ns at threshold; data setup time, 20 ns; hold time, zero.

Pattern and Delayed Trigger Outputs

High: ≥2 V into 50Ω (line driver interface).
Low: <0.4 V into 50Ω (line driver interface).
Pulse duration
Delayed trigger: ≈ 25 ns (RZ format) at 1 V level.
Pattern trigger: ≈ 25 ns in RZ format at 1 V level, delay zero or off. With delay on and not zero, pattern trigger output starts on receipt of a pattern trigger signal and ends when delay ends.

Trigger Arm Input

Impedance: 50Ω.
Level: low state, 0 V to <0.4 V; high state, 2 V to <5 V.
Pulse width: 15 ns min at 1.5 V level.
Arming conditions: if the arming pulse positive edge occurs <45 ns after a clock, triggering occurs on the same clock cycle that it is armed. If the arming pulse positive edge occurs >75 ns after a clock, triggering occurs on the next clock cycle.

1607A X-, Y- and Z-axes Outputs

X-axis: <0.6 V to >6 V p-p, ±8 V max into ≥100 kΩ
Y-axis: <0.6 V to >6 V p-p, ±8 V max into ≥100 kΩ.
Z-axis: 0 to 10 V p-p into ≥1 kΩ.
Display interface requirements: the 1607A interfaces with oscilloscope or display with the following input parameters (Not recommended for storage oscilloscopes or displays other than HP Model 1741 Opt 001 Storage Oscilloscope).
X and Y inputs: 0.1 to 1 V/div deflection factors; dc coupled input; and >500 kHz bandwidth.
Z-axis input: dc coupled with positive blanking; full blanking must occur with 10 V input at 10 mA.

General

Display rate: variable from <200 ms to >5 s (1600A), <50 ms to >5 s (1607A).
Power: 100, 120, 220, 240 Vac; −10%, +5%; 48 to 440 Hz; 120 VA max.
Logic probe power: rear panel BNC connector, +5V, 100 mA.
Size
1600A: 197 H x 335 W x 540 mm L with handle ($7^{3}/_{4}$″ x $13^{3}/_{16}$″ x $21^{1}/_{4}$″); 460 mm ($18^{1}/_{8}$″) L without handle.
1607A: 121 H x 284 W x 460 mm D ($4^{3}/_{4}$″ x $11^{3}/_{16}$″ x $18^{1}/_{8}$″).
Operating environment: temperature, 0 to +55°C (+32°F to +130°F); humidity to 95% relative humidity at +40°C (+104°F); altitude to 4600 m (15 000 ft); vibrated in three planes for 15 minutes each with 0.254 mm (0.010 in.) excursion, 10 to 55 Hz.
Weight
1600S: net, 19.1 kg (42 lb); shipping, 22.7 kg (50 lb).
1600A: net, 12.7 kg (28 lb); shipping, 15.9 kg (35 lb).
1607A: net, 6.4 kg (14 lb); shipping, 8.2 kg (18 lb).

Accessories supplied
1600S: six 10231C data probes, two 10230C clock probes, one 10236A Trigger Bus Cable, one 10237A Data Cable, two 2.3. m (7.5 ft) power cords, one accessory case for each analyzer, one 1600A and one 1607A Operating and Service Manual.
1600A or 1607A: three 10231C data probes, one 10230C clock probe, one accessory case, one Operating and Service Manual.

10253A Specifications

Cards: printed cards in format required for 1600A Logic State Analyzer Table B memory; 187 mm (7⅜″) long.
Power: supplied by 1600A.
Weight: net, 1 kg (2.1 lb); shipping, 1.8 kg (4 lb).
Operating environment: same as 1600A except: temperature, +10°C to +40°C (+50°F to +104°F); humidity, to 80% relative humidity at +40°C (+104°F).
Accessories supplied: one drum card, HP P/N 10253-90001; one exerciser card, HP P/N 10253-90002; 100 data cards, HP P/N 9320-3324; one interface box mounting bracket, HP P/N 01120-64701; and one Operating Note.

10254A Specifications

Probe Inputs

Rep rate: ≤10 MHz in Edge Sync, ≤7MHz in Pattern Sync.
Input RC: 40 kΩ ± 3kΩ shunted by ≤14 pF (at the probe tip).
Input threshold: TTL, fixed at 1.5 Vdc; variable ± 10 Vdc selected at the logic state analyzer.
Max Input: level, ±15 Vdc; swing, 15 V peak from threshold.
Min Input: pulse width, 40 ns min at threshold; setup time, 50 ns min; hold time, zero.

Operating Modes

Display format
Bits/byte: 1 to 16 bits (a byte is one line on the display).
First bit, left/right: displays most significant bit left or right.
Data sync
Pattern: sync on selected unique pattern in the serial data stream.
Edge: sync on input signal on selected edge.
Bytes/sync: select from 1 to 16 bytes of data following each sync.
Delay: 1 to 99 clock pulses after sync signal before data acquisition begins.
Sync search: Initiate pushbutton or a positive-going input pulse starts a new search cycle.

General

Weight: net, 3.2 kg (7 lb.). Shipping, 5 kg (11 lb).
Power: supplied by the 1600A or 1607A.
Size: 12.1 H × 28.4 W × 41.4 cm D ($4^{3}/_{4}$ × $11^{3}/_{16}$″ × $16^{5}/_{16}$″).
Accessories supplied: one Model 10236A Trigger Bus Cable, four interface cables (HP P/N 10254-61601), and one Operating Note.

Ordering Information

	Price
1600S 32-channel Logic State Analyzer, includes a 1600A and 1607A	$7100
Opt 910: extra set of manuals	add $35
1600A 16-channel Logic State Analyzer	$4200
Opt 910: extra Operating and Service Manual	add $18
1607A 16-channel Logic State Analyzer	$2900
Opt 910: extra Operating and Service Manual	add $17
10253A Card Reader	$800
10254A Serial-to-parallel Converter	$1275